XC3000 Series
Field Programmable Gate Arrays
(XC3000A/L, XC3100A/L)

November 9, 1998 (Version 3.1)

Product Description

Features

- Complete line of four related Field Programmable Gate Array product families
  - XC3000A, XC3000L, XC3100A, XC3100L
- Ideal for a wide range of custom VLSI design tasks
  - Replaces TTL, MSI, and other PLD logic
  - Integrates complete sub-systems into a single package
  - Avoids the NRE, time delay, and risk of conventional masked gate arrays
- High-performance CMOS static memory technology
  - Guaranteed toggle rates of 70 to 370 MHz, logic delays from 7 to 1.5 ns
  - System clock speeds over 85 MHz
  - Low quiescent and active power consumption
- Flexible FPGA architecture
  - Compatible arrays ranging from 1,000 to 7,500 gate complexity
  - Extensive register, combinatorial, and I/O capabilities
  - High fan-out signal distribution, low-skew clock nets
  - Internal 3-state bus capabilities
  - TTL or CMOS input thresholds
  - On-chip crystal oscillator amplifier
- Unlimited reprogrammability
  - Easy design iteration
  - In-system logic changes
- Extensive packaging options
  - Over 20 different packages
  - Plastic and ceramic surface-mount and pin-grid-array packages
  - Thin and Very Thin Quad Flat Pack (TQFP and VQFP) options
- Ready for volume production
  - Standard, off-the-shelf product availability
  - 100% factory pre-tested devices
  - Excellent reliability record
- Complete Development System
  - Schematic capture, automatic place and route
  - Logic and timing simulation
  - Interactive design editor for design optimization
  - Timing calculator
  - Interfaces to popular design environments like Viewlogic, Cadence, Mentor Graphics, and others

Additional XC3100A Features

- Ultra-high-speed FPGA family with six members
  - 50-85 MHz system clock rates
  - 190 to 370 MHz guaranteed flip-flop toggle rates
  - 1.55 to 4.1 ns logic delays
- High-end additional family member in the 22 X 22 CLB array-size XC3195A device
- 8 mA output sink current and 8 mA source current
- Maximum power-down and quiescent current is 5 mA
- 100% architecture and pin-out compatible with other XC3000 families
- Software and bitstream compatible with the XC3000, XC3000A, and XC3000L families

XC3100A combines the features of the XC3000A and XC3100 families:

- Additional interconnect resources for TBUFs and CE inputs
- Error checking of the configuration bitstream
- Soft startup holds all outputs slew-rate limited during initial power-up
- More advanced CMOS process

Low-Voltage Versions Available

- Low-voltage devices function at 3.0 - 3.6 V
- XC3000L - Low-voltage versions of XC3000A devices
- XC3100L - Low-voltage versions of XC3100A devices

Device	Max Logic Gates	Typical Gate Range	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3020A, 3020L, 3120A	1,500	1,000 - 1,500	64	8 x 8	64	256	16	14,779
XC3030A, 3030L, 3130A	2,000	1,500 - 2,000	100	10 x 10	80	360	20	22,176
XC3042A, 3042L, 3142A, 3142L	3,000	2,000 - 3,000	144	12 x 12	96	480	24	30,784
XC3064A, 3064L, 3164A	4,500	3,500 - 4,500	224	16 x 14	120	688	32	46,064
XC3090A, 3090L, 3190A, 3190L	6,000	5,000 - 6,000	320	16 x 20	144	928	40	64,160
XC3195A	7,500	6,500 - 7,500	484	22 x 22	176	1,320	44	94,984