

Features

- Optimized for high-performance 2.5V systems
 - 5 ns pin-to-pin logic delays
 - Small footprint packages including VQFPs, TQFPs and CSPs (Chip Scale Package)
 - Lower power operation
 - Multi-voltage operation
 - FastFLASH technology
- Advanced system features
 - In-system programmable
 - Output banking (XC95144XV, XC95288XV)
 - Superior pin-locking and routability with Fast CONNECT™ II switch matrix
 - Extra wide 54-input Function Blocks
 - Up to 90 product-terms per macrocell with individual product-term allocation
 - Local clock inversion with three global and one product-term clocks
 - Individual output enable per output pin with local inversion
 - Input hysteresis on all user and boundary-scan pin inputs
 - Bus-hold circuitry on all user pin inputs
 - Full IEEE Standard 1149.1 boundary-scan (JTAG) support on all devices
- Four pin-compatible device densities
 - 36 to 288 macrocells, with 800 to 6400 usable gates
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
 - 20 year data retention
 - ESD protection exceeding 2,000V
- Pin-compatible with 3.3V core XC9500XL family in common package footprints
- Hot Plugging capability

Family Overview

The XC9500XV family is a 2.5V CPLD family targeted for high-performance, low-voltage applications in leading-edge communications and computing systems, where high device reliability and low power dissipation is important. Each XC9500XV device supports in-system programming (ISP) and the full IEEE 1149.1 (JTAG) boundary-scan, allowing superior debug and design iteration capability for small form-factor packages. The XC9500XV family is designed to work closely with the Xilinx Spartan™-XL and Virtex™ FPGA families, allowing system designers to partition logic optimally between fast interface circuitry and high-density general purpose logic. As shown in [Table 1](#), logic density of the XC9500XV devices ranges from 800 to 6400 usable gates with 36 to 288 registers, respectively. Multiple package options and associated I/O capacity are shown in [Table 2](#). The XC9500XV family members are fully pin-compatible, allowing easy design migration across multiple density options in a given package footprint.

The XC9500XV architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. In-system programming throughout the full commercial operating range and a high programming endurance rating provide worry-free reconfigurations of system field upgrades. Extended data retention supports longer and more reliable system operating life.

Advanced system features include output slew rate control and user-programmable ground pins to help reduce system noise. Each user pin is compatible with 3.3V and 2.5V inputs, and the outputs may be configured for 3.3V, 2.5V, or 1.8V operation. The XC9500XV device exhibits symmetric full 2.5V output voltage swing to allow balanced rise and fall times.

Architecture Description

Each XC9500XV device is a subsystem consisting of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the Fast CONNECT II switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capability with extra wide 54 inputs and 18 outputs. The Fast CONNECT II switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, up to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs. See [Figure 1](#).