

**Features**

- High-speed: 35, 70 ns
- Ultra low DC operating current of 5mA (max.)
- Low Power Dissipation:
  - TTL Standby: 3 mA (Max.)
  - CMOS Standby: 20  $\mu$ A (Max.)
- Fully static operation
- All inputs and outputs directly compatible
- Three state outputs
- Ultra low data retention current ( $V_{CC} = 2V$ )
- Single  $5V \pm 10\%$  Power Supply

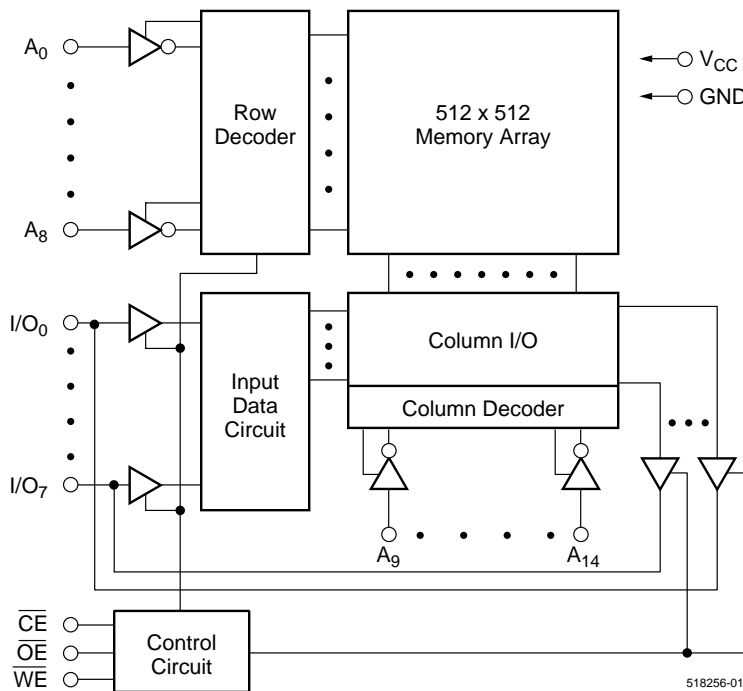
■ Packages

- 28-pin TSOP (Standard)
- 28-pin 600 mil PDIP
- 28-pin 330 mil SOP (450 mil pin-to-pin)

**Description**

The V62C518256 is a 262,144-bit static random access memory organized as 32,768 words by 8 bits. It is built with MOSEL VITELIC's high performance CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

**Functional Block Diagram**



**Device Usage Chart**

Operating Temperature Range	Package Outline			Access Time (ns)		Power		Temperature Mark
	T	P	F	35	70	L	LL	
0°C to 70 °C	•	•	•	•	•	•	•	Blank
-40°C to +85°C	•	•	•	•	•	•	•	I