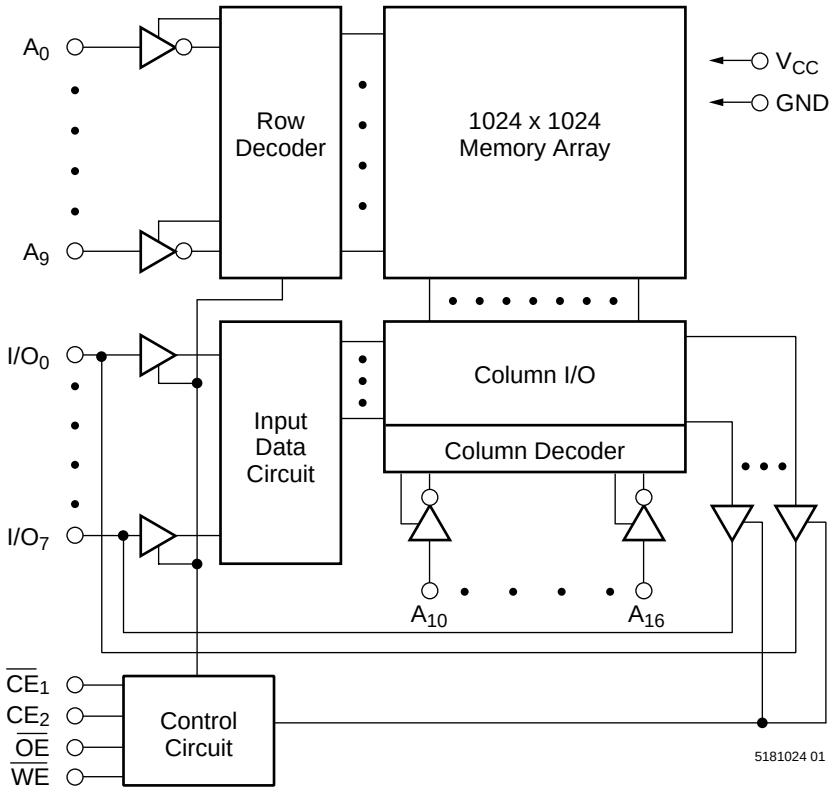
Features

- High-speed: 35, 70 ns
- Ultra low DC operating current of 5mA (max.)
  - TTL Standby: 5 mA (Max.)
  - CMOS Standby: 60 µA (Max.)
- Fully static operation
- All inputs and outputs directly compatible
- Three state outputs
- Ultra low data retention current (V_{CC} = 2V)
- Single 5V ± 10% Power Supply
- Packages
  - 32-pin TSOP (Standard)
  - 32-pin 600 mil PDIP
  - 32-pin 440 mil SOP (525 mil pin-to-pin)

Description

The V62C5181024 is a 1,048,576-bit static random-access memory organized as 131,072 words by 8 bits. It is built with MOSEL VITELIC's high performance CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Functional Block Diagram



Device Usage Chart

Operating Temperature Range	Package Outline			Access Time (ns)		Power		Temperature Mark
	T	W	P	35	70	L	LL	
0°C to 70 °C	•	•	•	•	•	•	•	Blank
–40°C to +85°C	•	•	•	•	•	•	•	I