ADVANCED INFORMATION

MX29F200T/B

2M-BIT [256Kx8/128Kx16] CMOS FLASH MEMORY

FEATURES

- 5.0V±10% for read, erase and write operation
- 131072x16/262144x8 switchable
- Fast access time: 55/70/90/120ns
- Low power consumption
  - 40mA maximum active current@5MHz
  - 1uA typical standby current
- Command register architecture
  - Byte/Word Programming (7us/12us typical)
  - Erase (16K-Bytex1, 8K-Bytex2, 32K-Bytex1, and 64K-Byte x3)
- Auto Erase (chip) and Auto Program
  - Automatically erase any combination of sectors or the whole chip with Erase Suspend capability.
  - Automatically program and verify data at specified address
- Status Reply
  - Data polling & Toggle bit for detection of program and erase cycle completion.
- Ready/Busy pin(RY/BY)
  - Provides a hardware method or detecting program or erase cycle completion
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Sector protect/unprotect for 5V only system or 5V/12V system
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Boot Code Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Low VCC write inhibit is equal to or less than 3.2V
- Package type:
  - 44-pin SOP
  - 48-pin TSOP
- Erase suspend/ Erase Resume
  - Suspends an erase operation to read data from, or program data to a sector that is not being erased, then resume the erase operation.
- Hardware RESET pin
  - Resets internal state mechine to the read mode
- 20 years data retention

GENERAL DESCRIPTION

The MX29F200T/B is a 2-mega bit, single 5 Volt Flash memory organized as 1M word x16 or 2M bytex8 MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F200T/B is packaged in 44-pin SOP and 48-pin TSOP. It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

The standard MX29F200T/B offers access time as fast as 55ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29F200T/B has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29F200T/B uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29F200T/B uses a 5.0V ± 10% VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.