



# PALCE24V10H-15/25

## EE CMOS 28-Pin Universal Programmable Array Logic

### DISTINCTIVE CHARACTERISTICS

- Electrically erasable CMOS technology provides reconfigurable logic and full testability
- High speed CMOS technology
  - 15 ns propagation delay for "-15" version
  - 25 ns propagation delay for "-25" version
- Outputs individually programmable as registered or combinatorial
- Programmable output polarity
- Programmable enable/disable control
- Preloadable output registers for testability
- Automatic register reset on power-up
- Cost-effective 28-pin plastic SKINNYDIP and PLCC packages
- Extensive third-party support through FusionPLD partners
- Fully tested for 100% programming and functional yields and high reliability

### GENERAL DESCRIPTION

The PALCE24V10 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. Its macrocells provide a universal device architecture.

The PALCE24V10 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be pro-

grammed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE24V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

### BLOCK DIAGRAM

