



MAX 3000A

Programmable Logic Device Family

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Data Sheet

Features...

- High-performance, low-cost CMOS EEPROM-based programmable logic devices (PLDs) built on a MAX[®] architecture (see [Table 1](#))
- 3.3-V in-system programmability (ISP) through the built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface with advanced pin-locking capability
 - ISP circuitry compliant with IEEE Std. 1532
- Built-in boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990
- Enhanced ISP features:
 - Enhanced ISP algorithm for faster programming
 - ISP_Done bit to ensure complete programming
 - Pull-up resistor on I/O pins during in-system programming
- High-density PLDs ranging from 600 to 10,000 usable gates
- 4.5-ns pin-to-pin logic delays with counter frequencies of up to 227.3 MHz
- MultiVolt[™] I/O interface enabling the device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), plastic J-lead chip carrier (PLCC), and FineLine BGA[™] packages
- Hot-socketing support
- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- Industrial temperature range

Table 1. MAX 3000A Device Features

Feature	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	34	66	98	161	208
t _{PD} (ns)	4.5	4.5	5.0	7.5	7.5
t _{SU} (ns)	2.9	2.8	3.3	5.2	5.6
t _{CO1} (ns)	3.0	3.1	3.4	4.8	4.7
f _{CNT} (MHz)	227.3	222.2	192.3	126.6	116.3