Agilent Technologies
Innovating the HP Way

Optically Coupled 20 mA Current Loop Transmitter

Technical Data

HCPL-4100

Features

- **Guaranteed 20 mA Loop Parameters**
- **Data Input Compatible with LSTTL, TTL and CMOS Logic**
- **Guaranteed Performance over Temperature (0°C to 70°C)**
- **Internal Shield for High Common Mode Rejection**
- **20 kBaud Data Rate at 400 Metres Line Length**
- **Guaranteed On and Off Output Current Levels**
- **Safety Approval**
  UL Recognized -2500 V rms for 1 minute
  CSA Approved
- **Optically Coupled 20 mA Current Loop Receiver, HCPL-4200, Also Available**

Applications

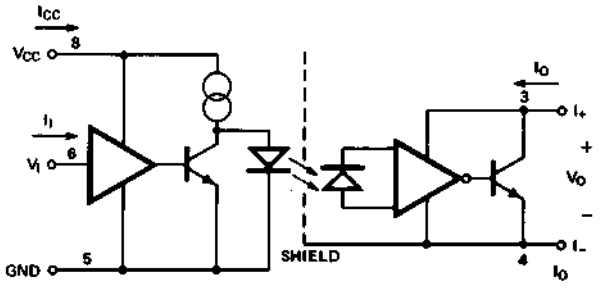
- **Isolated 20 mA Current Loop Transmitter in:**
  Computer Peripherals
  Industrial Control Equipment
  Data Communications Equipment

Description

The HCPL-4100 optocoupler is designed to operate as a transmitter in equipment using the 20 mA current loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the logic input to the 20 mA current loop breaks ground loops and provides very high immunity to common mode interference.

The HCPL-4100 data input is compatible with LSTTL, TTL, or CMOS logic gates. The input integrated circuit drives a GaAsP LED. The light emitted by the LED is sensed by a second integrated circuit that allows 20 mA to pass with a voltage drop of less than 2.7 volts when no light is emitted and allows less than 2 mA to pass when light is emitted. The transmitter output is capable of withstanding 27 volts. The input integrated circuit provides a controlled amount of LED drive current and takes into account any LED light output degradation. The internal shield allows a guaranteed 1000 V/µs common mode transient immunity.

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)*

VI	VCC	IO
H	ON	H
L	ON	L
H	OFF	H
L	OFF	H

*CURRENT LOOP CONVENTION —
H = MARK: $I_O \geq 12$ mA,
L = SPACE: $I_O \leq 2$ mA.

A 0.1 µF bypass capacitor connected between pins 8 and 5 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.