RT54SX-S
RadTolerant FPGAs for Space Applications

Special Features for Space

- First Actel FPGA Designed Specifically for Space Applications
- Up to 2,012 Additional SEU Hardened Flip-Flops Eliminate Software TMR Necessity (LETth > 40, GEO SEU Rate < 10^{-10} upset/bit-day)
- Up to 100krad (Si) Total Ionizing Dose (TID) Parametric Performance Supported with Lot-Specific Test Data
- Single Event Latch-Up Immune
- Flexible I/O Accommodates 2.5V, 3.3V, and 5.0V Input Signals
- Pin Compatibility Allows Prototyping with Commercial SX-A FPGAs, and Mission Implementation with Radiation-Tolerant RT54SX-S
- Deterministic Power-Up
- No Sequencing Required for Supply Voltages at Power-Up
- Cold Sparing Capability
- Devices Available from TM1019.5-tested Pedigreed Lots
- 5.0V CMOS Input Trip Point Option

Standard Features

- Very Low Power Consumption (Up to 68 mW at Standby)
- Configurable I/O Support for 3.3V/5.0V PCI, LVTTL, TTL Levels, and CMOS
- 2.5V, 3.3V, and 5.0V Mixed Voltage Operation
- 5.0V Input Tolerance and 5.0V Drive Strength
- Hot-Swapping Capability
- QML Certified Devices
- Secure Programming Technology Prevents Reverse Engineering and Design Theft
- Configurable Weak Resistor Pull-up or Pull-down for Tristated Outputs at Power-Up
- 100% Circuit Resource Utilization with 100% Pin Locking
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Dedicated JTAG Reset (TRST) Pin
- Deterministic, User-Controllable Timing
- JTAG Boundary Scan Testing In Compliance with IEEE Standard 1149.1
- CMOS Latch-Up Immunity
- 0.25µm Metal-to-Metal Antifuse Process Generation

Leading Edge Performance

- 250 MHz System Performance
- 8.9 ns Clock-to-Out (Pin-to-Pin)
- 310 MHz Internal Performance

Specifications

- 48,000 to 108,000 Available System Gates
- Up to 360 User-Programmable I/O Pins (package dependent)

RT54SX-S Product Profile

Device	RT54SX32S	RT54SX72S
Capacity		
Typical Gates	32,000	72,000
System Gates	48,000	108,000
Logic Modules	2.880	6,036
Combinatorial Cells	1,800	4,024
SEU Hardened Register Cells (Dedicated Flip-Flops)	1,080	2,012
Maximum Flip-Flops	1,980	4,024
Maximum User I/Os	227	212
Clocks	3	3
Quadrant Clocks	0	4
Clock-to-Out	8.9 ns	11.0 ns
Input Set-Up (External)	–1.3 ns	–3.3 ns
Speed Grades	Std, –1	Std, –1
Package (by pin count)		
CQFP	208, 256	208, 256